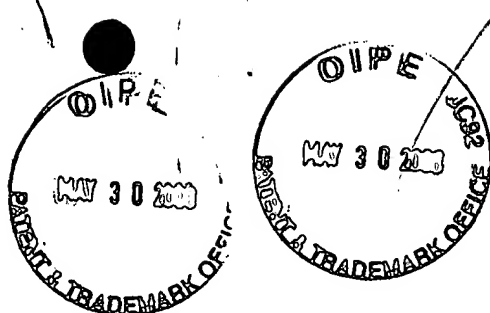


MEGIC-99-005



May 26, 2000

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To: Commissioner of Patents and Trademarks  
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572  
20 McIntosh Drive  
Poughkeepsie, N.Y. 12603

Subject:

Serial No. 09/523,990 03/13/00

Mou-Shiung Lin, Chien-Hsun Lee

METHOD OF MANUFACTURE AND IDENTI-  
FICATION OF SEMICONDUCTOR CHIP  
MARKED FOR IDENTIFICATION WITH  
INTERNAL MARKING INDICIA AND PRO-  
TECTION THEREOF BY NON-BLACK LAYER  
AND DEVICE PRODUCED THEREBY

Grp. Art Unit: 2876

#### INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation  
In An Application.

The following Patents and/or Publications are submitted to  
comply with the duty of disclosure under CFR 1.97-1.99 and  
37 CFR 1.56. Copies of each document is included herewith.

~~U.S. Patent 5,641,997 to Ohta et al., "Plastic-~~  
Encapsulated Semiconductor Device", describes encapsulating a  
semiconductor device between plastic sheets. The plastic is  
formed of resins which have colorants.

U.S. Patent 5,973,395 to Suzuki et al., "IC Package Having a Single Wiring Sheet with a Lead Pattern Disposed Thereon", describes an IC package that has a flexible wiring sheet, including an upper portion, a lower portion and a side portion which is wound around a base member over an upper surface, side surfaces and a lower surface of the base member.

A paper by John Baliga, "Ball Grid Arrays: The High-Pincount Workhorse", Semiconductor International, September 1999, pp. 1-2, discusses how most microprocessors, graphics chips and ASICs are packaged in ball grid array (BGA) packages. These devices have too many I/Os to use a peripherally leaded package on the board, and thermal requirements that cannot be handled by a CSP or direct chip attach. Moving to flip-chip attach inside the package has both economic and performance advantages, but is still only used for higher-performance applications.

U.S. Patent 4,300,184 to Colla, "Conformal Coating for Electrical Circuit Assemblies", discusses a transparent coating over a printed circuit system including circuit conductors, resistors and transistors permitting visual inspection of the circuit as well as convenient cutting or removal of the coating for access to the circuit.

A paper by John Baliga, "Defining the CSP", Chip Scale Technology, September 1999, pp. 6-8, discusses the various types of chip scale packages.

U.S. Patent 5,461,545 to Leroy et al., "Process and Device for Hermetic Encapsulation of Electronic Components", discusses plastic packages which enclose electronic components which contain discrete components or integrated electronic components encapsulated in the packages, which can be mounted flat.

U.S. Patent 5,479,049 to Aoki et al., "Solid State Image Sensor Provided with a Transparent Resin Layer Having Water Repellency and Oil Repellency and Flattening a Surface Thereof", discusses a solid state image sensor device containing light sensors formed in the surface of a semiconductor.

U.S. Patent 5,834,340 to Sawai et al., "Plastic Molded Semiconductor Package and Method of Manufacturing the Same", discusses how a pad electrode is formed on a main surface of a semiconductor chip.

U.S. Patent 5,866,949 to Schueller, "Chip Scale Ball Grid Array for Integrated Circuit Packaging", discusses a chip scale ball grid array for integrated circuit packaging having a non-polymer layer or support structure positioned between a semiconductor die and a substrate.

U.S. Patent 5,925,934 to Lim, "Low Cost and Highly Reliable Chip-Sized Package", discusses a chip-sized package (CSP) and method for making a CSP which is simple to manufacture, less costly and more compact, thus being truly a chip-sized package.

U.S. Patent 5,951,804 to Kweon et al., "Method for Simultaneously Manufacturing Chip-Scale Package Using Lead Frame Strip with a Plurality of Lead Frames", discloses a method for simultaneously manufacturing chip-scale packages employing a lead frame strip having a plurality of lead frames.

U.S. Patent 5,955,784 to Chiu, "Ball Contact for Flip-Chip Device", discusses a contact for a semiconductor device or passive substrate which is made up of an array of conductive balls, the individual balls of the contact being a compressible material coated with a metal conductive material.

U.S. Patent 5,970,321 to Hively, "Method of Fabricating a Microelectronic Package Having Polymer ESD Protection", discusses a semiconductor package having positioned therein a protection layer which protects the integrated circuit chip from electrostatic discharge (ESD) damage. Contact leads are formed in a pair of opposing rows on the upper surface of the base tape.

Sincerely,



Stephen B. Ackerman, Reg.# 37761